Decoder für RAM und ROM

U5121 74F521

U5122 74ACT138

U5123 74F521

U5124A 74ACT139

Decoder für I/O

U5201 74F521

U5202 74F521

U5203 74F521

U5204 74F521

U5205 74F138

U5206 74F138

Unbenutzte Elemente

U5124B 74ACT139

U5101C 74F00

U5101D 74F00

U5110B 74F20

RAM

U5131 AS6C4008

U5132 AS6C4008

U5133 AS6C4008

U5134 AS6C4008

U5135 AS6C4008

U5136 AS6C4008

U5137 AS6C4008

U5138 AS6C4008

ROM

U5139 DS1245 / AT27C010

U5140 DS1245 / AT27C010

U5141 DS1245 / AT27C010

U5142 DS1245 / AT27C010

U5143 DS1245 / AT27C010

U5144 DS1245 / AT27C010

U5145 DS1245 / AT27C010

U5146 DS1245 / AT27C010

Interface für Display und Keyboard (Zeitmultiplex)

U5221 74F273

U5222 74F374

U5223 74F245

J5221 CON40

RN5221 8X10KSIL

Status- und Debugausgabe

DIS_5221 5082_7340

DIS_5222 5082_7340

Versorgung und Entkopplung

CAS101–CAS146 0.1uF

CAT5101–CAT5106 10uF 20V

R5101 1K

R5103 1K

BR5101 0R0

BR5102 0R0

BR5103 0R0

Pegelanpassung für RAM und ROM

U5101A 74F00

U5110A 74F20

U5101B 74F00

U5102 74ACT245

U5103 74ACT245

U5104 74ACT245

U5105 74ACT245

U5106 74ACT245

U5107 74ACT245

U5108 74ACT245

U5109 74ACT245

Nachverdrahtung

RN?? 8X1K5IL

Speicher I/O (Erweiterung)

J5101 VG96ABC =VME J1/P1

J5102 VG96ABC =VME J2/P2

TiGRIS Elektronik GmbH
Wikingerufer 7
10555 Berlin, Germany
Tel: +49 (30) 301048-30
Web: http://www.tigris.eu
Mail: info@tigris.eu

Title	SPACE AGE 2 CPU	Speicher und I/O-Schnittstelle SP2-001 MEM_IO	
Size A1	Document Number: TiGRIS Artikel-Nummer:		Rev 1.20
Date: Wednesday, September 16, 2015		Sheet 1 of 14	

Debug-Zugriff auf Speicher-Daten

Daten von und zu RAM

U3821 74ACT652 — U3822 74ACT652 — U3823 74ACT652 — U3824 74ACT652

debug_d0 … debug_d15 ↔ mem_d0 … mem_d15

mbdebug_wr_mem_d_B0 … mbdebug_wr_mem_d_B3

debug_to_mem_d

mbdebug_wr_mem_d_B0 … mbdebug_wr_mem_d_B3

CLKAB, CLKBA, OEAB, OEBA, SAB, SBA

U3825A 74ACT74 — D, CLK, WRITE, HALT, Q — debug_to_mem_d

mbdebug_wr_dbug_to_mem_d — mmem — H2

Bidirektionaler Multiplexer

U3101 … U3116 74F245 — A0…A7 / B0…B7, OE, DIR

mem_d0 … mem_d15 ↔ mig_d0 … mig_d15

dbug_to_mem

mux_memdb1_mig01

Vorzeichenerweiterung für lh und lb

U3117 74F245 — U3118 74F245 — U3119 74F245

sign — H2

sign_extend_B1 — sign_extend_B2 — sign_extend_B3/B0

mig_d0 … mig_d31

RN2101 … RN2104 — 8X330K — VCC

Steuerung für Vorzeichenerweiterung

U2154A 74F00 — mxdr = lb or lbu — sign_extend_B1

mreg_to_mem

U2154B 74F00 — mxdr = lb or lbu or lh or lhu — sign_extend_B2/B3

U2155A 74F08 — mig_d7, xsel = lb

U2156A 74F32 — mig_d15, xsel = lh — U2155B 74F08

"Einspeisung" für Daten vom Register zum externen Speicher

Daten vom Speicher zu Register

Daten von Register zu Speicher

U3130 74F245 — U3121 74F245 — U3122 74F245 — U3123 74F245

mig_d0 … mig_d31 ↔ mig_out_d_B0 … mig_out_d_B3

mreg_to_mem

Steuerung für bidirektionalen Multiplexer

U2145D 74F00 — U2147A 74F00 — U2148A 74F00 — U2148B 74F00 — U2148C 74F00 — U2145C 74F00 — U2148D 74F00 — U2147B 74F00 — U2148E 74F00 — U2147C 74F00 — U2147D 74F00

mxdr = lw/ or sw/ — subaddress = 1

mxdr = lw/ or sw/ — subaddress = 2

mxdr = lb or lbu or sb — subaddress = 3

mxdr = lb or lbu or sb — subaddress = 0

mxdr = lw/ or sw/ — subaddress = 0

mxdr = lb or lbu or sb — subaddress = 2

mxdr = lw/ or sw/ — subaddress = 1

mxdr = lb or lbu or sb — subaddress = 1

mxdr = lw/ or sw/ — subaddress = 3

mxdr = lw/ or sw/ — subaddress = 0

mxdr = lb or lbu or sb — subaddress = 2

BR2106 0R0 — BR2107 0R0 — BR2101 0R0 — BR2103 0R0 — BR2102 0R0 — BR2104 0R0 — BR2105 0R0

mxm_mem8bit_reg80 … mxm_mem8bit_reg83

U2152 74F30 — U2154C 74F08 — U2153A 74F21 — U2153B 74F21 — U2150A 74F08 — U2150B 74F21 — U2150C 74F08 — U2150D 74F08 — U2151A 74F32 — U2151B 74F32 — U2151C 74F32 — U2151D 74F32

mxm_mem80_reg80 … mxm_mem83_reg83

Bildung der Schreibsignale für Speicher und Register und des Lesesignals für den Speicher

Bildung Schreibsignale für Register

mxm_mem8bit_reg80 … mxm_mem8bit_reg83

U2157 74F30 — U2158 74F30 — U2165 74F30 — U2166 74F30

mxdr = lb or lbu or lh or lhu

wr_wr_B0 … wr_wr_B3

Schreibsignale (Freigabe) für Register

Bildung Schreibsignale für externen Speicher

U2163A 74F08 — U2163B 74F08 — U2164A 74F32 — U2164B 74F32

mxm_mem8bit_reg80 … mxm_mem8bit_reg83

wr_wr_mem_B0 … wr_wr_mem_B3

Bildung Schreibsignale für externen Speicher

U2150A 74F08 — U2150B 74F08 — U2150C 74F08 — U2150D 74F08

mem_wr

wr_wr_mem_B0 … wr_wr_mem_B3

Bildung Lesesignale für externen Speicher

U2826 74F257 — U2827 74F257

mem_oe_mc

debug_wr_mem_wr

debug_to_mem_ctrl

Output-Enable für RAM, ROM, IO

Steuersignale für externen Speicher

Daten-Multiplexer

J2001 VG96A40C — +VME 210P1

mem_d0 … mem_d31 ↔ mig_d0 … mig_d31

clk

mxsel

d_mem_wr0 … d_mem_wr3

wr_wr_B0 … wr_wr_B3

mxsel_wr_mc

mem_oe

dbus_en_ea_to_mem

J2002 VG96A40C — +VME 220P1

mig_d0 … mig_d31

mig_out_d_B0 … mig_out_d_B3

mig_out_d_B0 … mig_out_d_B3

mig_out_d_B0 … mig_out_d_B3

mig_out_d_B0 … mig_out_d_B3

mig_out_d_B0 … mig_out_d_B3

dbug_wr_dbug_to_mem_d

dbug_wr_mem_d_B0 … dbug_wr_mem_d_B3

dbug_wr_mem_d_B0 … dbug_wr_mem_d_B3

Decodierung der Befehle

mxdr[31..26]

dbus_en_ea_to_mem

mxdr[31..26] — mxdr[25..21] — mxdr[20..16] — mxdr[15..11] — mxdr[10..6] — mxdr[5..0]

U2134A 74F04 … U2134F 74F04

mxdr31 … mxdr26

U2162 74F30 — U2133 74F30 — U2134 74F30 — U2135 74F30 — U2136 74F30 — U2137 74F30 — U2138 74F30 — U2139 74F30 — U2140 74F30 — U2141 74F30

U2150C 74F08 — 101110 swr

U2143A 74F04 — mig_to_mem — TP2101 — mreg_to_mem

U2143B 74F04 … U2143F 74F04

101110 lwr, 101110 lwl — 101111 bwr, 101111 bwl — 101100 sh — 101000 sb — 101001 sh — 100000 lb — 100001 lh

U2154A 74F04 — U2154C 74F00 — U2154D 74F04 — U2154B 74F00 — U2155B 74F08 — mxdr = lb or lbu or sb — mxdr = lb or lbu or sb or lhu — mxdr = lb or lbu — TP2102 — mxdr = lh

U2144A 74F04 — mxdr = lb — mxdr = lh

Decodierung der Subadressen

U2125A 74F139 — U2126A 74F04 … U2126D 74F04

subaddress = 0 … subaddress = 3

Abnahme RAM-Adresse von ALU (hinter Register ALU_S bzw.p Zwischenteil

Decoder für Debug-Selectsignale

U2829 74ACT138 — U2830 74ACT138

debug_wd_dmux

debug_sl_mem_sl_B0 … debug_sl_mem_sl_B3

debug_sl_mem_sh_B0 … debug_sl_mem_sh_B3

Debug-und Downloadzugriff auf Ext. RAM und ROM (NVRAM)

U2828 74ACT273 — U2156B 74F04

debug_sl_mem_sl0 … debug_sl_mem_sl3

debug_sl_mem_sh0 … debug_sl_mem_sh3

debug_sl_mem_ctrl

Schreibsignale für RAM und I/O und für ROM-Download

Entkopplung

CA2101 … CA2171 0.1uF

CAT2101 … CAT2105 10uF 20V

Statische Pegel

R2101 1K — R2102 1K — RNV1 1K — VCC — H1 — H2 — H3

BR2111 0R0 — BR2112 0R0 — L1 — L2

Unbenutzte Elemente

U2826 74F257 — U2827 74F257 — U2829 74ACT138 — U2830 74ACT138 — U2828 74ACT273 — U2156B 74F04 — U2144F 74F04 — U2154D 74F00 — U2150C 74F08 — U2150D 74F08 — U2156B 74F32 — U2156C 74F32

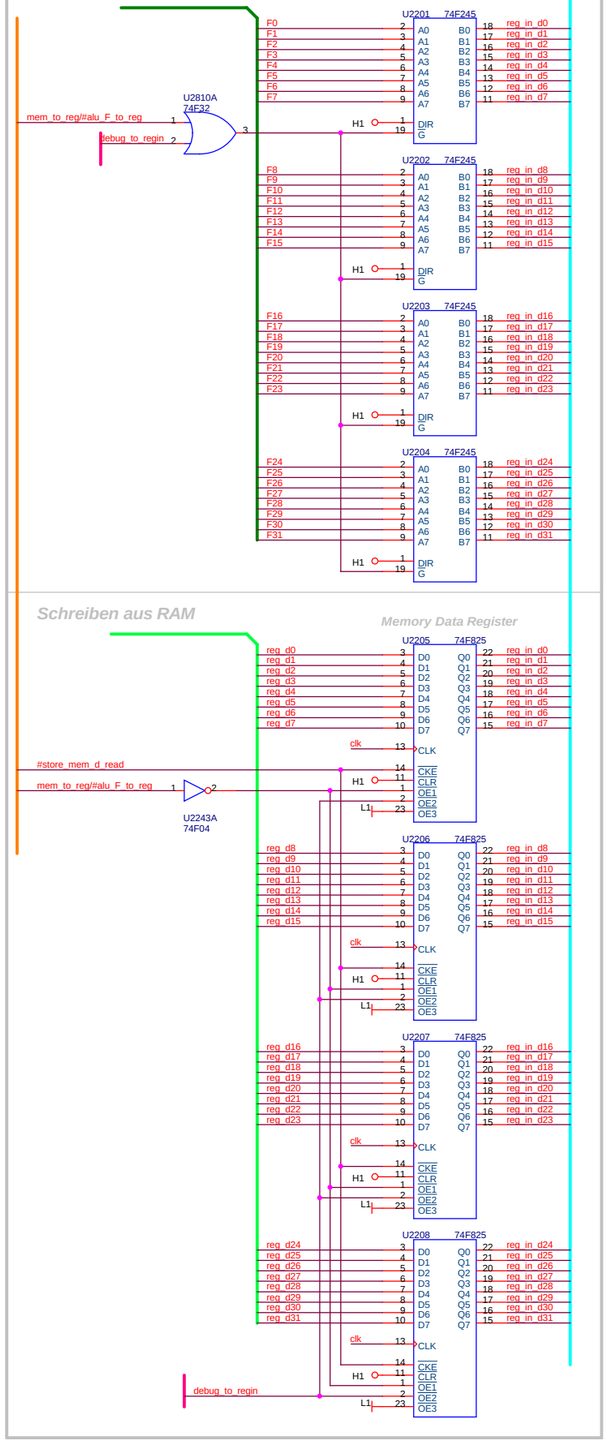
Nachvendefahrung in Netzebene des Schaltplans eingepflegt

TGRIS Elektronik GmbH
Wilmingerufer 7
10555 Berlin, Germany
Tel.: +49 (30) 301048-30
Web: http://www.tgris.eu
Mail: info@tgris.eu

Title:	RPACE AGE 2 CPU — Daten-Multiplexer MEM DATA MUX
Size: A0	Document Number: TGRIS Artikel-Nummer: — Rev: 0.2.0
Date:	Wednesday, September 16, 2015 — Sheet 2 of 14

Daten-Multiplexer Schreiben

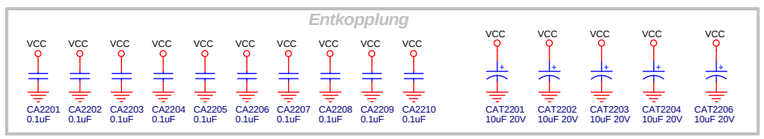
Schreiben ALU-Ergebnis



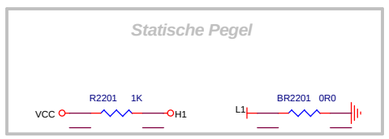
Schreiben aus RAM

Memory Data Register

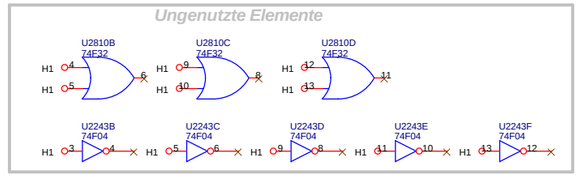
Entkopplung

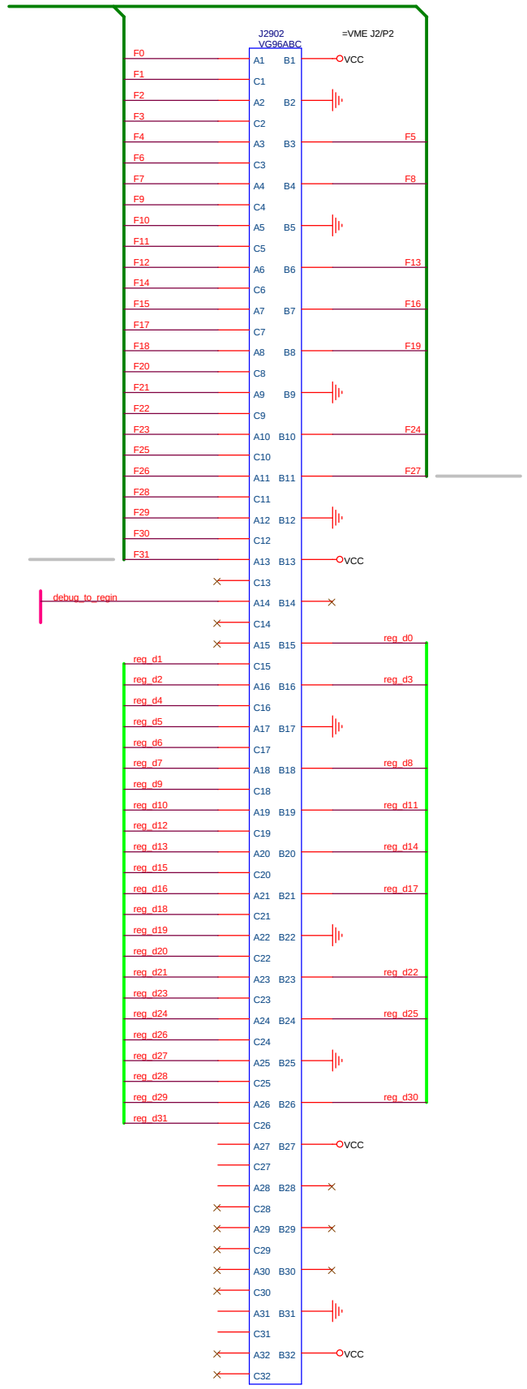


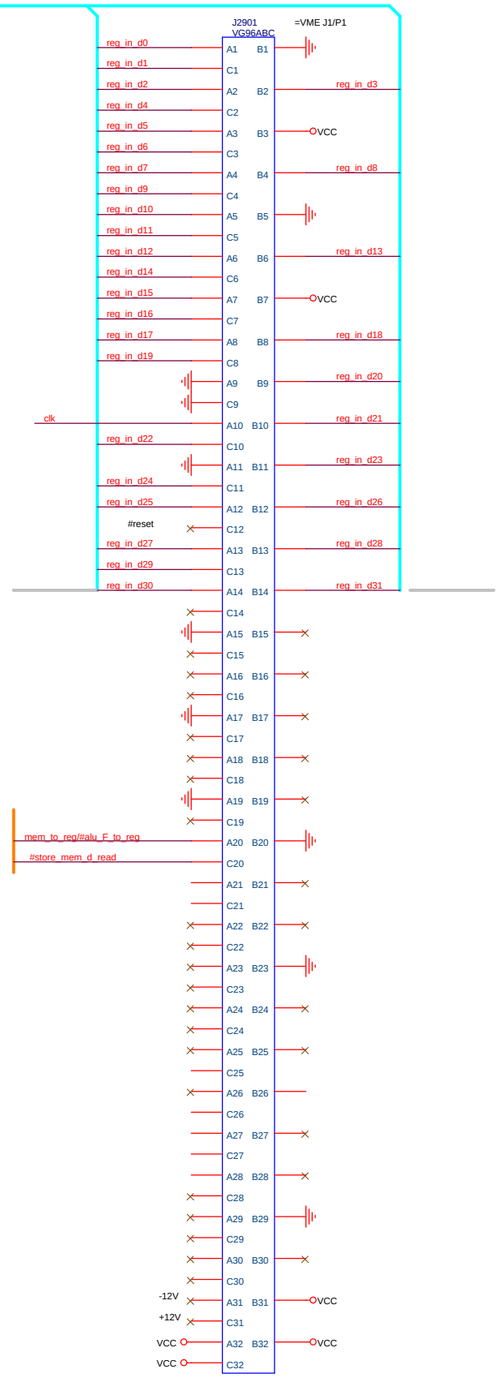
Statische Pegel



Ungenutzte Elemente







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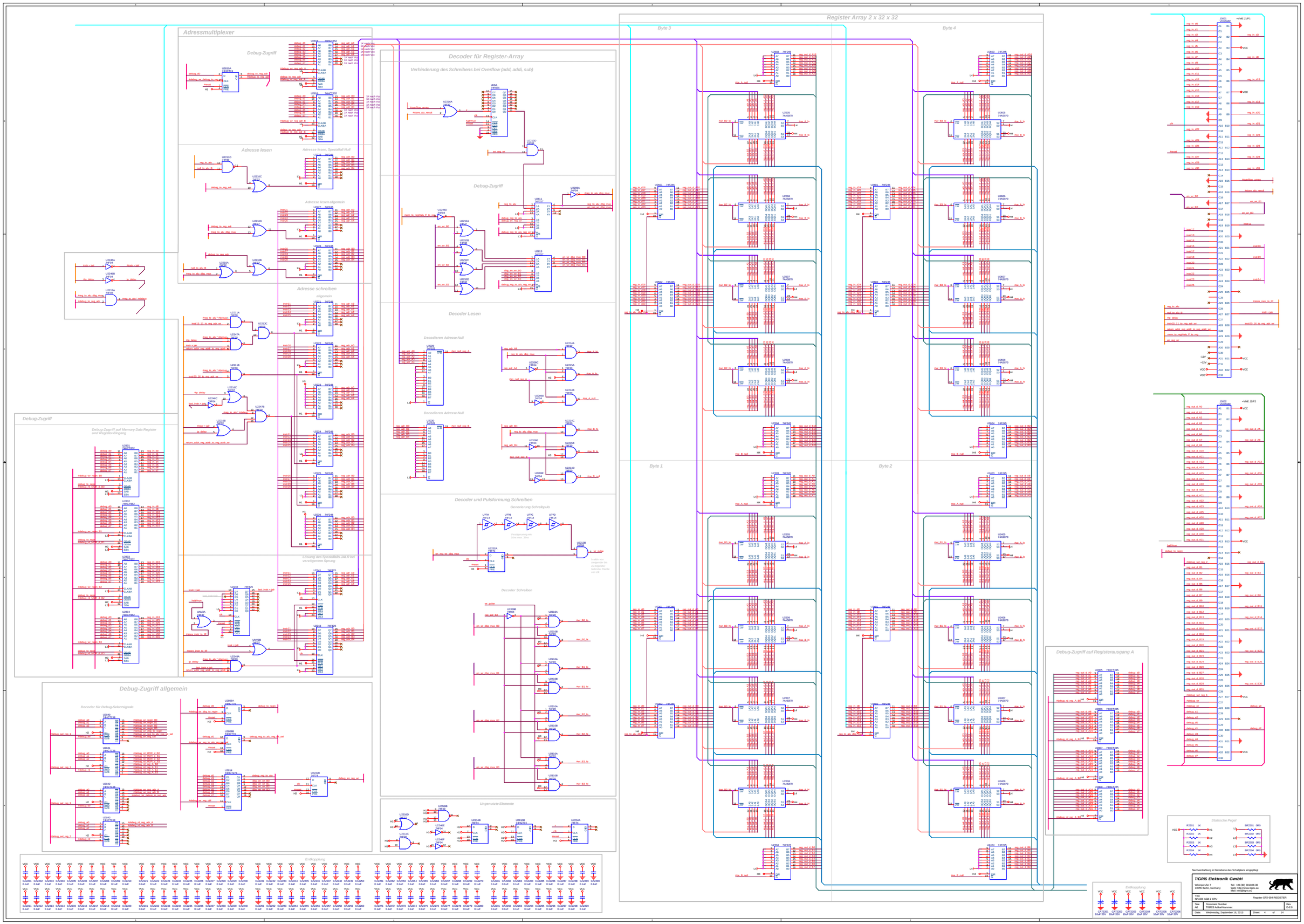
Title: SPACE AGE 2 CPU	Datenmultiplexer für Register SP2-003 REG DATA MUX	
Size: A2	Document Number: TIGRIS Artikel-Nummer:	Rev: 1.20
Date: Wednesday, September 16, 2015	Sheet 3 of 14	


Adressmultiplexer
Debug-Zugriff
Adresse lesen
Adresse lesen, Spezialfall Null
Adresse lesen allgemein
Adresse schreiben
allgemein
Debug-Zugriff
Debug-Zugriff auf Memory Data Register und Register-Eingang
Lösung des Spezialfalls JALR bei verzögertem Sprung
Debug-Zugriff allgemein
Decoder für Debug-Selectsignale
Decoder für Register-Array
Verhinderung des Schreibens bei Overflow (add, addi, sub)
Debug-Zugriff
Decoder Lesen
Decodieren Adresse Null
Decodieren Adresse Null
Decoder und Pulsformung Schreiben
Generierung Schreibpuls
Decoder Schreiben
Ungenutzte Elemente
Entkopplung
Register Array 2 x 32 x 32
Byte 3
Byte 4
Byte 1
Byte 2
Debug-Zugriff auf Registerausgang A
Statische Pegel
Entkopplung
Nachverdrahtung in Netzebene des Schaltplans eingepflegt
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10555 Berlin, Germany
Tel: +49 (30) 3010/49-30
Web: http://www.tigris.eu
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SPACE AGE 2 CPU
Register SP2-004 REGISTER
Size
A0
Document Number
TIGRIS Artikel-Nummer:
Rev
D-2.0
Date
Wednesday, September 16, 2015
Sheet
4
of
14

PC >> 2

-4 für Berechnung Rücksprung nach Exception

U2701 74F245
U2702 74F245
U2703 74F245
U2704 74F245
U2705 74F245
U2706 74F245
U2707 74F245
U2708 74F245
U2791 74F245
U2792 74F245
U2793 74F245
U2794 74F245

#PC_to_alu_A
#reg_to_alu_A
#-4_to_alu_A

Decodierung Ansteuerung ALU-Eingangsmultiplexer

U2717 74F138
src_alu_A_0
src_alu_A_1
src_alu_A_2
#PC_to_alu_A
#reg_to_alu_A
#lo_to_alu_A
#hi_to_alu_A
#-4_to_alu_A

R2701 1K
BR2701 0R0

J2702 VG96ABC =VME J2/P2

J2701 VG96ABC =VME J1/P1

CA2701 0.1uF
CA2702 0.1uF
CA2703 0.1uF
CA2704 0.1uF
CA2705 0.1uF
CA2706 0.1uF
CA2707 0.1uF
CA2708 0.1uF
CA2709 0.1uF
CA2710 0.1uF
CA2711 0.1uF
CA2712 0.1uF
CA2713 0.1uF

CAT2701 10uF 20V
CAT2702 10uF 20V
CAT2703 10uF 20V
CAT2704 10uF 20V
CAT2706 10uF 20V

Nachverdrahtung in Netzebene des Schaltplans eingepflegt

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Wikingerufer 7
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Tel: +49 (30) 301048-30
Web: http://www.tigris.eu
Mail: info@tigris.eu

Title: SPACE AGE 2 CPU	ALU-Eingangsmultiplexer A SP2-005 ALU_A_MUX	
Size: A2	Document Number: TIGRIS Artikel-Nummer:	Rev: D-2.0
Date: Wednesday, September 16, 2015	Sheet 5 of 14	

Exception Program Counter EPC

Exception Program Counter EPC geeloppelt für Debug-Zugriff

Eingangsmultiplexer ALU_B

Verwendung für Imm und Offset

Decoder für Debug-Selectsignale

VME J1/P1

VME J2/P2

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Wikingerufer 7
10555 Berlin, Germany
Tel: +49 (30) 301048-30
Web: http://www.tigris.eu
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Title	SPACE AGE 2 CPU	ALU-Eingangsmultiplexer B SP2-006 ALU_B_MUX	
Size: A3	Document Number: TiGRIS Artikel Nummer:		Rev: 1.20
Date: Wednesday, September 16, 2015	Sheet 6 of 14		

Operandenregister für softwareemulierte Befehle

Operandenregister mul/div A

U2920 74F138
mul_div_S0
mul_div_S1
mul_div_S2
H1
#store_reg_to_mul_div
L1
#store_operand_A8
#store_operand_A8
#store_reg_to_lo
#store_reg_to_hi
clk
H1
L1
U2902 74F825
U2903 74F825
U2904 74F825
U2905 74F825
alu_in_A0 … alu_in_A31
mem_d0 … mem_d31
Auslesen über lw aus dem I/O-Bereich
#op_A_to_mem

Operandenregister mul/div B

U2906 74F825
U2907 74F825
U2908 74F825
U2909 74F825
alu_in_B0 … alu_in_B31
mem_d0 … mem_d31
Auslesen über lw aus dem I/O-Bereich
#op_B_to_mem

Register LO schreibend

#store_reg_to_lo
#lo_to_alu_A
U2921 74F825
U2922 74F825
U2923 74F825
U2924 74F825
alu_in_A0 … alu_in_A31

Register HI schreibend

#store_reg_to_hi
#hi_to_alu_A
U2925 74F825
U2926 74F825
U2927 74F825
U2928 74F825
alu_in_A0 … alu_in_A31

J2601 VG96ABC =VME J1/P1
mem_d0 … mem_d31
clk
#reset
#hi_to_alu_A
#lo_to_alu_A
mul_div_S0
mul_div_S1
mul_div_S2
#store_reg_to_mul_div
#op_A_to_mem
#op_B_to_mem

J2602 VG96ABC =VME J2/P2
alu_in_B0 … alu_in_B31
#debug_sel_mu_div
#debug_wr
#debug_rd
debug_a1
debug_a2
debug_d0 … debug_d7
debug_a0
debug_d2

-12V
+12V
VCC

CA2901 … CA2917 0.1uF
CAT2901 … CAT2906 10uF 20V
R2951 1K
BR2951 0R0

Nachverdrahtung in Netzebene des Schaltplans eingepflegt

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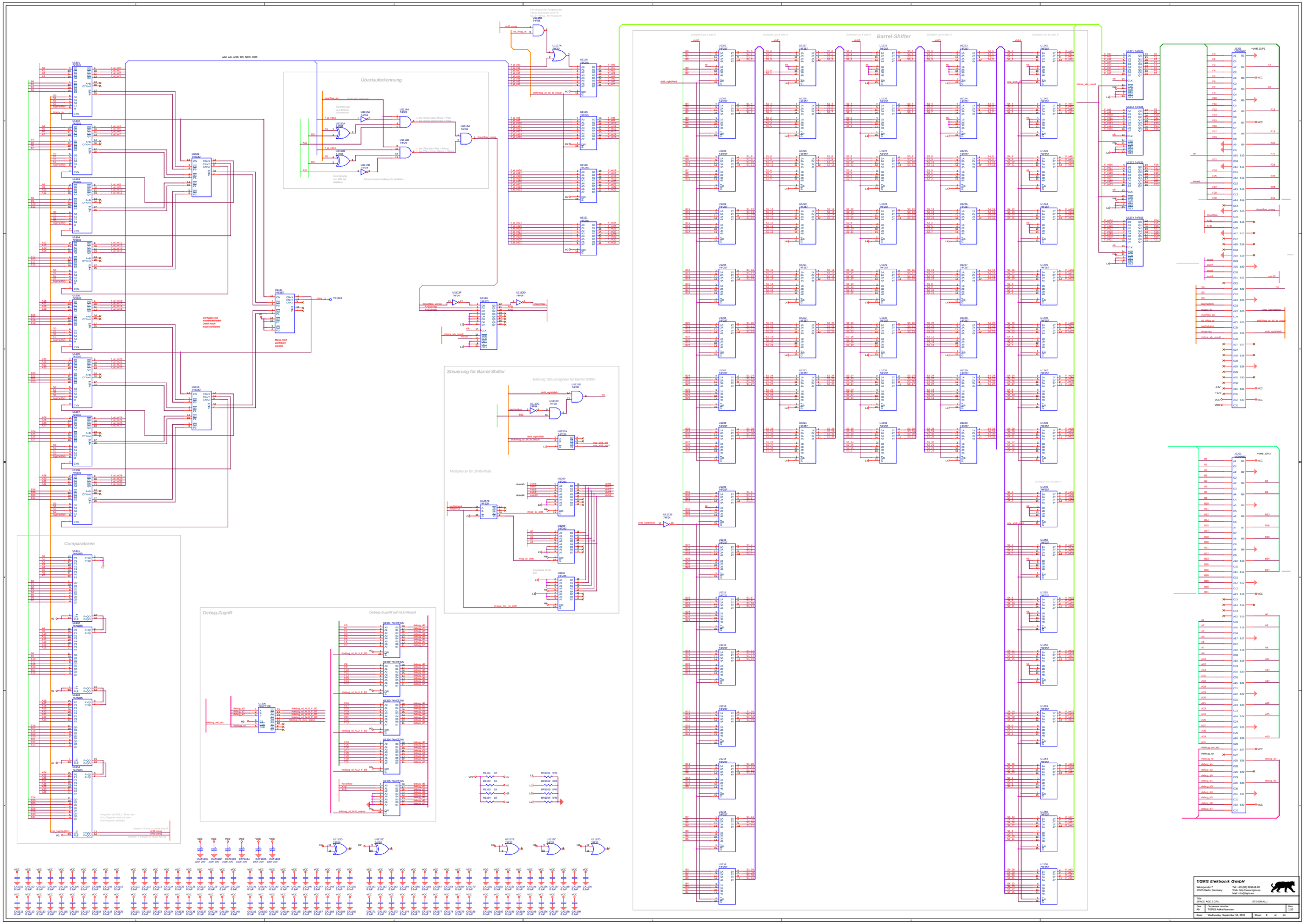
Size: A1	Document Number: TIGRIS Artikel-Nummer:	Rev: D-2.0
Date: Wednesday, September 16, 2015	Sheet 7 of 14	


Überlauferkennung
Barrel-Shifter
Steuerung für Barrel-Shifter
Bildung Steuersignale für Barrel-Shifter
Multiplexer für Shift-Weite
Comparatoren
Debug-Zugriff
Debug-Zugriff auf ALU-Result
TIGRIS Elektronik GmbH
Wilmersdorfer 7
10555 Berlin, Germany
Tel: +49 (30) 301049-30
Web: http://www.tigris.eu
Mail: info@tigris.eu
Title
SPACE AGE 2 CPU
SP2-008 ALU
Size
A0
Document Number
TIGRIS Artikel-Nummer
Rev
1.20
Date: Wednesday, September 16, 2015
Sheet 8 of 14

Zwischenspeichern der Sprungadresse

Program Counter PC

Multiplexer für Adresse zu externem Speicher

Sprungadresse (Jump)

Sprungadresse (Branch)

Bypass für Register mit 4 x 74_245 für unverzögerten Sprung

Multiplexerzweig für Interruptvektor

Debug-Zugriff auf Register PC

Debug-Zugriff auf Speicher-Adresse

Debug-Zugriff auf PC-Load

Decoder für Debug-Selectsignale

Breakpoint

Jumper für Debug-Betrieb

Adresse zu ROM/RAM und I/O

Nachverdrahtung in Netzebene des Schaltplans eingepflegt

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Wikingerufer 7
10555 Berlin, Germany
Tel: +49 (30) 201048-30
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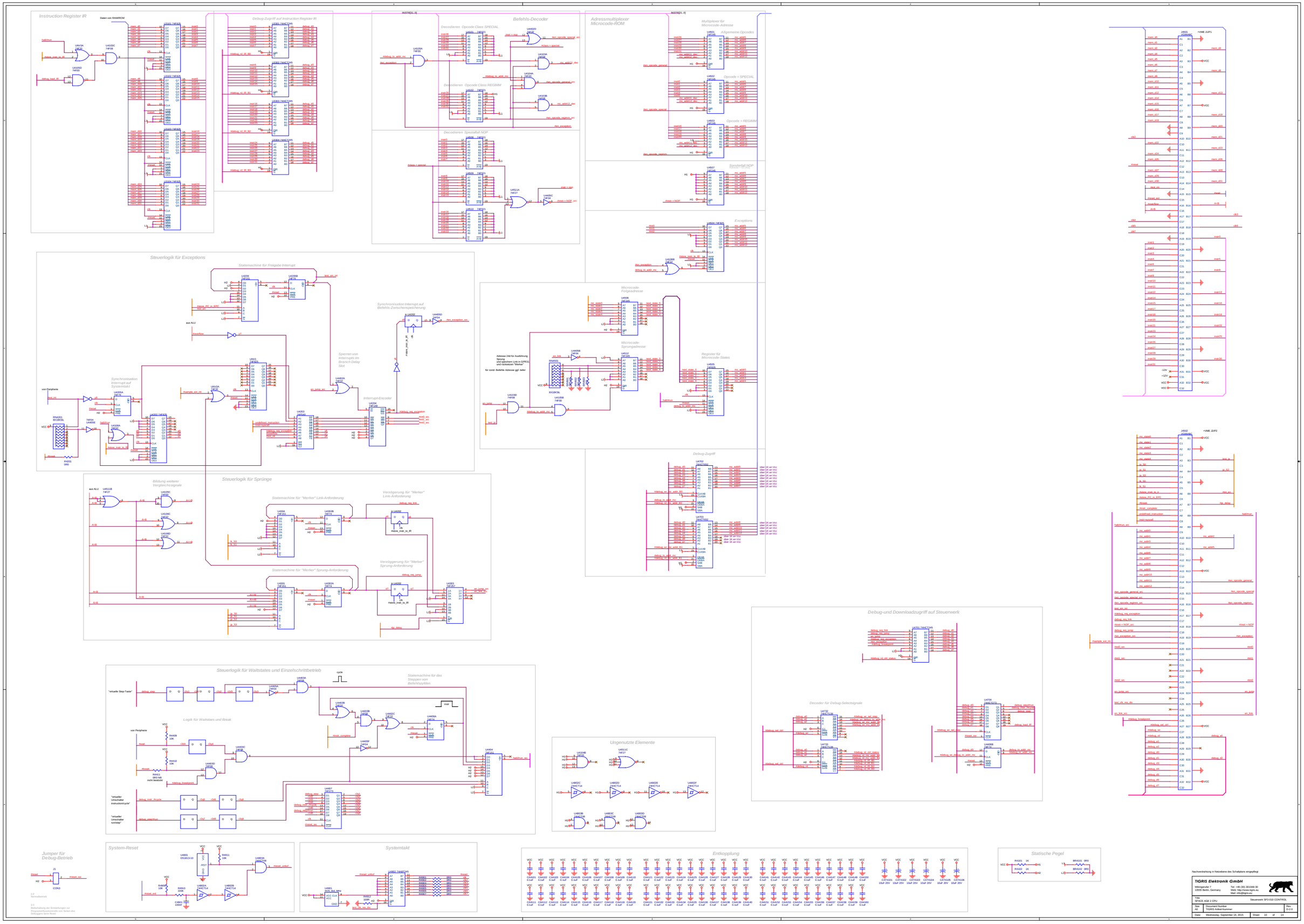
Title	SPACE AGE 2 CPU	SP2-009 ADDR GEN	
Size: A0	Document Number: TiGRIS Artikel-Nummer:		Rev: 0.2.0
Date:	Wednesday, September 16, 2015	Sheet 9 of 14	


Instruction Register IR
Debug-Zugriff auf Instruction Register IR
Befehls-Decoder
Decodieren Opcode Class SPECIAL
Decodieren Opcode Class REGIMM
Decodieren Spezialfall NOP
Adressmultiplexer Microcode-ROM
Multiplexer für Microcode-Adresse
Allgemeine Opcodes
Opcode = SPECIAL
Opcode = REGIMM
Sonderfall NOP
Exceptions
Steuerlogik für Exceptions
Statemachine für Freigabe Interrupt
Synchronisation Interrupt auf Befehls-Zwischenspeicherung
Sperren von Interrupts im Branch Delay Slot
Synchronisation Interrupt auf Systemtakt
Interrupt-Encoder
Microcode-Folgeadresse
Microcode-Sprungadresse
Register für Microcode-States
Debug-Zugriff
Steuerlogik für Sprünge
Bildung weiterer Vergleichssignale
Statemachine für "Merker" Link-Anforderung
Verzögerung für "Merker" Link-Anforderung
Statemachine für "Merker" Sprung-Anforderung
Verzöggerung für "Merker" Sprung-Anforderung
Debug-und Downloadzugriff auf Steuerwerk
Decoder für Debug-Selectsignale
Steuerlogik für Waitstates und Einzelschrittbetrieb
Statemachine für das Steppen von Befehlszyklen
Logik für Waitstates und Break
Ungenutzte Elemente
Jumper für Debug-Betrieb
System-Reset
Systemtakt
Entkopplung
Statische Pegel
Nachverdrahtung in Netzebene des Schaltplans eingepflegt
TIGRIS Elektronik GmbH
Wikingerufer 7
10555 Berlin, Germany
Tel. +49 (30) 301049-30
Web: http://www.tigris.eu
Mail: info@tigris.eu
Title
SPACE AGE 2 CPU
Steuerwerk SP2-010 CONTROL
Size
A0
Document Number
TIGRIS Artikel-Nummer
Rev
D-2.0
Date: Wednesday, September 16, 2015
Sheet 10 of 14

INSTR[31..0]

Microcode ROM

U1803 … U1807 — 8Mx8CMOY-70PC1 / AT27C256

mc_addr0 … mc_addr18 (A0 … A18)

mc_data0 … mc_data7 (D0 … D7)

H1 — 10K — debug_to_mc_en — mc_oe

mc_data0 … mc_data7 → debug_d0 … debug_d7

mc_addr0 … mc_addr18 → debug_a0 … debug_a18

mc_oe → debug_oe

mc_we → debug_we

mc_data0 … mc_data7 → mc_data0_w … mc_data7_w

mc_addr0 … mc_addr18 → mc_addr0_w … mc_addr18_w

mc_oe → mc_oe_w

mc_we → mc_we_w

microprogram address

statemachine control
jump/branch/clock

memory address source selection
memory control signals

memory data mux direction

microprogram flow control

U1808 … U1812 — 8Mx8CMOY-70PC1 / AT27C256

mc_addr0 … mc_addr18 (A0 … A18)

mc_data0 … mc_data7 (D0 … D7)

H1 — 10K — debug_to_mc_en — mc_oe

mc_data0 … mc_data7 → mc_data0_w … mc_data7_w

mc_addr0 … mc_addr18 → mc_addr0_w … mc_addr18_w

mc_oe → mc_oe_w

mc_we → mc_we_w

interrupt vector

temporary address storage

input register control

exception handling control

U1813 … U1817 — 8Mx8CMOY-70PC1 / AT27C256

mc_addr0 … mc_addr18 (A0 … A18)

mc_data0 … mc_data7 (D0 … D7)

H1 — 10K — debug_to_mc_en — mc_oe

mc_data0 … mc_data7 → mc_data0_w … mc_data7_w

mc_addr0 … mc_addr18 → mc_addr0_w … mc_addr18_w

mc_oe → mc_oe_w

mc_we → mc_we_w

I²C load source selection

I²C function control

register data direction

program counter control

register control

U1818 … U1822 — 8Mx8CMOY-70PC1 / AT27C256

mc_addr0 … mc_addr18 (A0 … A18)

mc_data0 … mc_data7 (D0 … D7)

H1 — 10K — debug_to_mc_en — mc_oe

mc_data0 … mc_data7 → mc_data0_w … mc_data7_w

mc_addr0 … mc_addr18 → mc_addr0_w … mc_addr18_w

mc_oe → mc_oe_w

mc_we → mc_we_w

register write enable

register write address selection

register write data selection

register read address control

U1823 … U1827 — 8Mx8CMOY-70PC1 / AT27C256

mc_addr0 … mc_addr18 (A0 … A18)

mc_data0 … mc_data7 (D0 … D7)

H1 — 10K — debug_to_mc_en — mc_oe

mc_data0 … mc_data7 → mc_data0_w … mc_data7_w

mc_addr0 … mc_addr18 → mc_addr0_w … mc_addr18_w

mc_oe → mc_oe_w

mc_we → mc_we_w

ALU input selection

sign extension input IS

ALU output control

ALU function selection

ALU control

U1828 … U1832 — 8Mx8CMOY-70PC1 / AT27C256

mc_addr0 … mc_addr18 (A0 … A18)

mc_data0 … mc_data7 (D0 … D7)

H1 — 10K — debug_to_mc_en — mc_oe

mc_data0 … mc_data7 → mc_data0_w … mc_data7_w

mc_addr0 … mc_addr18 → mc_addr0_w … mc_addr18_w

mc_oe → mc_oe_w

mc_we → mc_we_w

M

function select: sel <=> logical, arithmetic

function select: shift <=> sel, logical, arithmetic

shift direction

shift amount source selection

U1833 … U1837 — 8Mx8CMOY-70PC1 / AT27C256

mc_addr0 … mc_addr18 (A0 … A18)

mc_data0 … mc_data7 (D0 … D7)

H1 — 10K — debug_to_mc_en — mc_oe

mc_data0 … mc_data7 → mc_data0_w … mc_data7_w

mc_addr0 … mc_addr18 → mc_addr0_w … mc_addr18_w

mc_oe → mc_oe_w

mc_we → mc_we_w

overflow detection enable (add, addi, sub)

comparator_control

debug control

U1838 … U1842 — 8Mx8CMOY-70PC1 / AT27C256

mc_addr0 … mc_addr18 (A0 … A18)

mc_data0 … mc_data7 (D0 … D7)

H1 — 10K — debug_to_mc_en — mc_oe

mc_data0 … mc_data7 → mc_data0_w … mc_data7_w

mc_addr0 … mc_addr18 → mc_addr0_w … mc_addr18_w

mc_oe → mc_oe_w

mc_we → mc_we_w

mul_div_s1

mul = ph

mul = lul

mul = sysstuff

sysstuff

undefined instruction

external interrupt

Downloadzugriff auf Microcode-ROM

U4708 … U4716 — 28HCT852

mc_state0 … mc_state7 → debug_d0 … debug_d7

mc_addr0 … mc_addr18 → debug_a0 … debug_a18

mc_oe → debug_oe

mc_we → debug_we

debug_to_mc_en → debug_to_mc

Buffer für Steuersignale

U4821 … U4828 — 74F245

mc_state0 … mc_state7 → mc_state0 … mc_state7

mc_addr0 … mc_addr18 → mc_addr0 … mc_addr18

mc_oe → mc_oe

mc_we → mc_we

debug_to_mc_en → OE

Interface für Debugger

Debug_Schnittstelle, vom/zu PC-Interface

VCC

R4801 10K

R4802 1K

C4801 1nF

U4809A 74HCT14

U4809B 74HCT14

debug_wr_ext → debug_wr

debug_d0 … debug_d7

debug_a0 … debug_a2

debug_rd

debug_wr

VCC

RN4801 8X10KOL

RN4802 8X10KOL

U4802 74HCT154

debug_a0 … debug_a3 → A, B, C, G1, G2

debug_rd → G2

debug_wr → G1

debug_sel_ctrl_1 … debug_sel_ctrl_4

debug_sel_mc_1 … debug_sel_mc_4

debug_sel_mc_ctrl

debug_sel_spare_1 … debug_sel_spare_4

Breite 300mil (LS-Altbestand)

decard nicht verwendet

Debug-und Downloadzugriff auf Microcode-ROM

Decoder für Debug-Selectsignale

U4720 … U4723 — 74HCT138

debug_a0 … debug_a3 → A, B, C

debug_rd → H2

debug_sel_mc_1 / debug_sel_mc_2 → G1

debug_wr → G2A, G2B

debug_sel_mc_1 → debug_sel_mc_1 … debug_sel_mc_4

debug_sel_mc_2 → debug_sel_mc_5 … debug_sel_mc_8

debug_wr → debug_sel_mc_ctrl

U4718 … U4724 — 74HCT273

debug_d0 … debug_d7 → D0 … D7

mreset → CLR

debug_sel_mc_1 / debug_sel_mc_2 → CLK

U4725A 74HCT74

debug_d0 → D

debug_to_d_mc → Q

mreset → CLR

debug_sel_debug_to_d_mc → CLK

H2 → PRE

U4726 … U4727 — 74HCT573

debug_d0 … debug_d7 → D0 … D7

mreset → OE

debug_sel_mc_ctrl → LE

U4717 … U4724 — 74HCT245

mc_data0 … mc_data7 → A0 … A7

debug_d0 … debug_d7 → B0 … B7

debug_to_d_mc → DIR

H2 → OE

Breite 300 mil LS-Altbestand

mc_ram_we

VCC

R4703 10K

J4701 CON2

Write Protect = Jumper offen
A14 = H für 27C256 = Jumper offen

Ungenutzte Elemente

U4809C 74HCT14 — H2 → 5

U4809D 74HCT14 — H2 → 9

U4809E 74HCT14 — H2 → 13

U4809F 74HCT14 — 11

U4728G 74F00 — H2, H2

U4725B 74HCT74 — H2, H2, H2, H2

Entkopplung

VCC — C4A801 … C4A810 — 0.1uF

VCC — C4B01 … C4B20 — 0.1uF

VCC — C4A01 … C4A04 — 10uF 20V

Statische Pegel

R4801 1K — VCC, H1

R4802 1K — H2

L1 — BR4801 BR3

Verbindungsstecker

J4601 — VG96/64C — +VME 2U/P1

J4702 — VG96/64C — +VME 2U/P2

mc_state0 … mc_state7

mc_addr0 … mc_addr18

VCC, +12V, -12V, VCC 0, VCC 0

Netzumbenennung in Netzsterne des Schaltplans eingepflegt

TiGRIS Elektronik GmbH
Wikingerufer 7
10555 Berlin, Germany
Tel: +49 (30) 39104B-30
Fax: +49 (30) 39104B-99
Mail: info@tigris.eu

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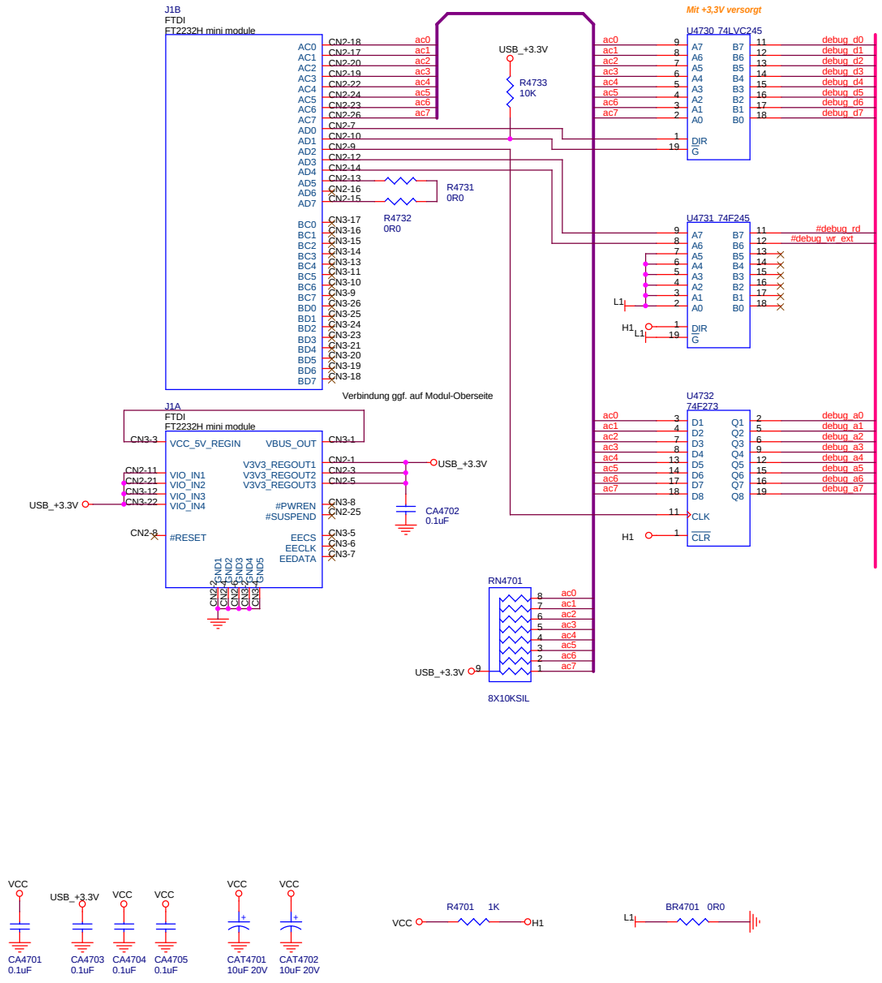
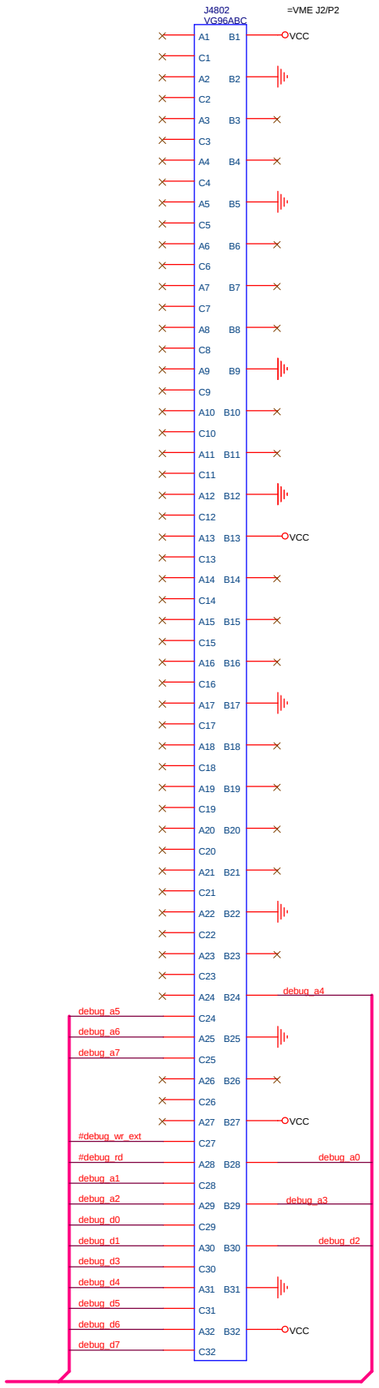
Title: SPACE-AGE 2 CPU	Microcode-ROM und Debug-Interface SP2-011 MICROCODE ROM	
Size: A0	Document Number: TiGRIS Artikel-Nummer	Rev: 0.2.0
Date: Wednesday, September 16, 2015	Sheet 11 of 14	





Nachverdrahtung in Netzebene des Schaltplans eingepflegt

TIGRIS Elektronik GmbH		
Wikingerufer 7 10555 Berlin, Germany	Tel: +49 (30) 301048-30 Web: http://www.tigris.eu Mail: info@tigris.eu	
Title SPACE AGE 2 CPU	USB-Interface (Debug) SP2-012 DEBUG HOST IF	
Size A2	Document Number TIGRIS Artikel-Nummer:	Rev D-2.0
Date: Wednesday, September 16, 2015	Sheet 12 of 14	

Speicher I/O (Erweiterung)

Speicher I/O (Erweiterung)

Speicher I/O (Video)

Speicher I/O (ROM/RAM)

Daten-Multiplexer

Daten-Multiplexer für Register

Register

ALU-Eingangsmultiplexer A

ALU-Eingangsmultiplexer B

Emulationsregister MUL/DIV

ALU

Adressgenerator

Steuerwerk ctrl/IR

Steuerwerk MC-ROM/Debug

Debug-Interface

Reset-Taster

Stromversorgung

TiGRIS Elektronik GmbH
Wikingerufer 7
10555 Berlin, Germany
Tel: +49 (30) 3910468-30
Web: http://www.tigris.eu
Mail: info@tigris.eu

Nachverdrahtung in Netzebene des Schaltplans eingepflegt

Title	SPACE AGE 2 CPU
	Backplane SP2-020 BACKPLANE
Size: A0	Document Number: TiGRIS Artikel-Nummer
Rev: 0.2.0	
Date: Wednesday, September 16, 2015	Sheet 13 of 14

Multiplex-Verbindung zum Rechner

J5401 CON40

R5401 1K

C5401 1nF

U5401A 74HCT14

U5401B 74HCT14

Display

LED_RAD_1 rt

LED_DEG_1 rt

LED_ERR_1 rt

R5402 220R

R5403 220R

R5404 220R

R5405 301R

R5406 301R

R5407 560R

DIS_V2_1 5082_7304

DIS_D7 5082_7300

DIS_D6 5082_7300

DIS_D5 5082_7300

DIS_D4 5082_7300

DIS_D3 5082_7300

DIS_D2 5082_7300

DIS_D1 5082_7300

DIS_D0 5082_7300

U5403 74ABT574

U5405B 74ABT244

U5405A 74ABT244

U5402 74HCT154_300mil

E 12345678

DEG RAD

log	ln	X^y	sin	cos	tan
10^x	e^x	$X^{1/y}$	sin^{-1}	cos^{-1}	tan^{-1}
1/X	X!	X^2	$\sqrt{}$	$\sqrt[3]{}$	D.R.
7	8	9	C	AC	ANS
4	5	6	X	÷	+/-
1	2	3	+	-	M in
0	.	EXP	=	M+	MR

Keyboard und Entprellung

4608X-102-224LF Bourns Mouser

RN5501A RN-SIL9_10K	RN5507A RN-SIL8_220K	C5501 0.1uF	U5501A 74HCT14	KEY_LOG_PRESSED
RN5502A RN-SIL9_10K	RN5508D RN-SIL8_220K	C5508 0.1uF	U5502B 74HCT14	KEY_LN_PRESSED
RN5503A RN-SIL9_10K	RN5510C RN-SIL8_220K	C5515 0.1uF	U5503C 74HCT14	KEY_XY_PRESSED
RN5504A RN-SIL9_10K	RN5512B RN-SIL8_220K	C5522 0.1uF	U5504D 74HCT14	KEY_SIN_PRESSED
RN5505A RN-SIL9_10K	RN5514A RN-SIL8_220K	C5529 0.1uF	U5505E 74HCT14	KEY_COS_PRESSED
RN5506A RN-SIL9_10K	RN5515D RN-SIL8_220K	C5536 0.1uF	U5506F 74HCT14	KEY_TAN_PRESSED
RN5501B RN-SIL9_10K	RN5507B RN-SIL8_220K	C5502 0.1uF	U5501B 74HCT14	KEY_10X_PRESSED
RN5502B RN-SIL9_10K	RN5509A RN-SIL8_220K	C5509 0.1uF	U5502C 74HCT14	KEY_EX_PRESSED
RN5503B RN-SIL9_10K	RN5510D RN-SIL8_220K	C5516 0.1uF	U5503D 74HCT14	KEY_X1/Y_PRESSED
RN5504B RN-SIL9_10K	RN5512C RN-SIL8_220K	C5523 0.1uF	U5504E 74HCT14	KEY_SIN-1_PRESSED
RN5505B RN-SIL9_10K	RN5514B RN-SIL8_220K	C5530 0.1uF	U5505F 74HCT14	KEY_COS-1_PRESSED
RN5506B RN-SIL9_10K	RN5516A RN-SIL8_220K	C5537 0.1uF	U5507A 74HCT14	KEY_TAN-1_PRESSED
RN5501C RN-SIL9_10K	RN5507C RN-SIL8_220K	C5503 0.1uF	U5501C 74HCT14	KEY_1/X_PRESSED
RN5502C RN-SIL9_10K	RN5509B RN-SIL8_220K	C5510 0.1uF	U5502D 74HCT14	KEY_X!_PRESSED
RN5503C RN-SIL9_10K	RN5511A RN-SIL8_220K	C5517 0.1uF	U5503E 74HCT14	KEY_X2_PRESSED
RN5504C RN-SIL9_10K	RN5512D RN-SIL8_220K	C5524 0.1uF	U5504F 74HCT14	KEY_V_PRESSED
RN5505C RN-SIL9_10K	RN5514C RN-SIL8_220K	C5531 0.1uF	U5506A 74HCT14	KEY_3V_PRESSED
RN5506C RN-SIL9_10K	RN5516B RN-SIL8_220K	C5538 0.1uF	U5507B 74HCT14	KEY_DR_PRESSED
RN5501D RN-SIL9_10K	RN5507D RN-SIL8_220K	C5504 0.1uF	U5501D 74HCT14	KEY_7_PRESSED
RN5502D RN-SIL9_10K	RN5509C RN-SIL8_220K	C5511 0.1uF	U5502E 74HCT14	KEY_8_PRESSED
RN5503D RN-SIL9_10K	RN5511B RN-SIL8_220K	C5518 0.1uF	U5503F 74HCT14	KEY_9_PRESSED
RN5504D RN-SIL9_10K	RN5513A RN-SIL8_220K	C5525 0.1uF	U5505A 74HCT14	KEY_C_PRESSED
RN5505D RN-SIL9_10K	RN5514D RN-SIL8_220K	C5532 0.1uF	U5506B 74HCT14	KEY_AC_PRESSED
RN5506D RN-SIL9_10K	RN5516C RN-SIL8_220K	C5539 0.1uF	U5507C 74HCT14	KEY_ANS_PRESSED
RN5501E RN-SIL9_10K	RN5508A RN-SIL8_220K	C5505 0.1uF	U5501E 74HCT14	KEY_4_PRESSED
RN5502E RN-SIL9_10K	RN5509D RN-SIL8_220K	C5512 0.1uF	U5502F 74HCT14	KEY_5_PRESSED
RN5503E RN-SIL9_10K	RN5511C RN-SIL8_220K	C5519 0.1uF	U5504A 74HCT14	KEY_6_PRESSED
RN5504E RN-SIL9_10K	RN5513B RN-SIL8_220K	C5526 0.1uF	U5505B 74HCT14	KEY_MUL_PRESSED
RN5505E RN-SIL9_10K	RN5515A RN-SIL8_220K	C5533 0.1uF	U5506C 74HCT14	KEY_DIV_PRESSED
RN5506E RN-SIL9_10K	RN5516D RN-SIL8_220K	C5540 0.1uF	U5507D 74HCT14	KEY_CHS_PRESSED
RN5501F RN-SIL9_10K	RN5508B RN-SIL8_220K	C5506 0.1uF	U5501F 74HCT14	KEY_1_PRESSED
RN5502F RN-SIL9_10K	RN5510A RN-SIL8_220K	C5513 0.1uF	U5503A 74HCT14	KEY_2_PRESSED
RN5503F RN-SIL9_10K	RN5511D RN-SIL8_220K	C5520 0.1uF	U5504B 74HCT14	KEY_3_PRESSED
RN5504F RN-SIL9_10K	RN5513C RN-SIL8_220K	C5527 0.1uF	U5505C 74HCT14	KEY_ADD_PRESSED
RN5505F RN-SIL9_10K	RN5515B RN-SIL8_220K	C5534 0.1uF	U5506D 74HCT14	KEY_SUB_PRESSED
RN5506F RN-SIL9_10K	RN5517A RN-SIL8_220K	C5541 0.1uF	U5507E 74HCT14	KEY_M_IN_PRESSED
RN5501G RN-SIL9_10K	RN5508C RN-SIL8_220K	C5507 0.1uF	U5502A 74HCT14	KEY_0_PRESSED
RN5502G RN-SIL9_10K	RN5510B RN-SIL8_220K	C5514 0.1uF	U5503B 74HCT14	KEY_DP_PRESSED
RN5503G RN-SIL9_10K	RN5512A RN-SIL8_220K	C5521 0.1uF	U5504C 74HCT14	KEY_EXP_PRESSED
RN5504G RN-SIL9_10K	RN5513D RN-SIL8_220K	C5528 0.1uF	U5505D 74HCT14	KEY_EQ_PRESSED
RN5505G RN-SIL9_10K	RN5515C RN-SIL8_220K	C5535 0.1uF	U5506E 74HCT14	KEY_M+_PRESSED
RN5506G RN-SIL9_10K	RN5517B RN-SIL8_220K	C5542 0.1uF	U5507F 74HCT14	KEY_MR_PRESSED

Ausleseschaltung für Keyboard

U5522 74HCT245

U5523 74HCT245

U5524 74HCT245

U5525 74HCT245

U5526 74HCT245

U5527 74HCT245

U5521 74HCT138

U5401C 74HCT14

U5401D 74HCT14

U5401E 74HCT14

U5401F 74HCT14

CA5401 CA5402 CA5403 CA5404 CA5405 CA5406 CA5407 CA5408 CA5409 CA5410 CA5411 CA5413 CA5414 CA5415 CA5416 CA5417 CA5418 CA5419 CA5420 CA5421 CA5422 CA5423 CA5424 CA5426 CA5427 CA5428 CA5429 CA5430 0.1uF

CAT5401 CAT5402 10uF 20V

RS499 1K

BR5401 0R0

Title	SPACE AGE 2 CPU — Anzeige und Keyboard SP2-030 I/O
Size	A1
Document Number	TIGRIS Artikel-Nummer:
Rev	1.20
Date	Wednesday, September 16, 2015
Sheet	14 of 14

TIGRIS Elektronik GmbH
Wikingerufer 7
10555 Berlin, Germany
Tel: +49 (30) 301048-30
Web: http://www.tigris.eu
Mail: info@tigris.eu