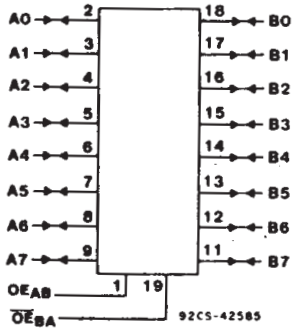
# CD54/74AC623
# CD54/74ACT623

Advance Information

TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS286A – October 2003




FUNCTIONAL DIAGRAM

## Octal-Bus Transceiver, 3-State, Non-Inverting

**Type Features:**

- *Buffered inputs*
- *Typical propagation delay: 4.5 ns @ $V_{CC}$ = 5 V, $T_A$ = 25°C, $C_L$ = 50 pF*

The RCA CD54/74AC623 and CD54/74ACT623 octal-bus transceivers use the RCA ADVANCED CMOS technology. They are non-inverting, 3-state, bidirectional transceiver-buffers that allow for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus, depending on the logic levels of the Output Enable ($OE_{AB}$, $\overline{OE}_{BA}$) inputs.

The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling $OE_{AB}$ and $\overline{OE}_{BA}$. Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high-impedance, both sets of bus lines will remain in their last states.

**The CD74AC623 is supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead small-outline packages (M, M96, and NSR suffixes). The CD74ACT623 is supplied in 20-lead small-outline packages (M96 suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (–40 to +85°C); and Extended Industrial/Military (–55 to +125°C).**

The CD54AC623 and CD54ACT623, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

**Family Features:**

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

**TRUTH TABLE**

| OUTPUT ENABLE INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}_{BA}$ | $OE_{AB}$ | |
| L | L | B DATA TO A BUS |
| H | H | A DATA TO B BUS |
| H | L | ISOLATION |
| L | H | B DATA TO A BUS, A DATA TO B BUS |

H = High level, L = Low level

Note: To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10 kΩ to 1 MΩ resistors.

This data sheet is applicable to the CD74AC623 and CD54/74ACT623. The CD54AC623 was not acquired from Harris Semiconductor.



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**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE ($V_{CC}$) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC $V_{CC}$ or GROUND CURRENT ($I_{CC}$ or $I_{GND}$) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For $T_A$ = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55 to +125°C
STORAGE TEMPERATURE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

**RECOMMENDED OPERATING CONDITIONS:**
**For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| Supply-Voltage Range, $V_{CC}$*: (For $T_A$ = Full Package-Temperature Range) | | | |
| AC Types | 1.5 | 5.5 | V |
| ACT Types | 4.5 | 5.5 | V |
| DC Input or Output Voltage, $V_I$, $V_O$ | 0 | $V_{CC}$ | V |
| Operating Temperature, $T_A$ | -55 | +125 | °C |
| Input Rise and Fall Slew Rate, dt/dv | | | |
| at 1.5 V to 3 V (AC Types) | 0 | 50 | ns/V |
| at 3.6 V to 5.5 V (AC Types) | 0 | 20 | ns/V |
| at 4.5 V to 5.5 V (ACT Types) | 0 | 10 | ns/V |

*Unless otherwise specified, all voltages are referenced to ground.

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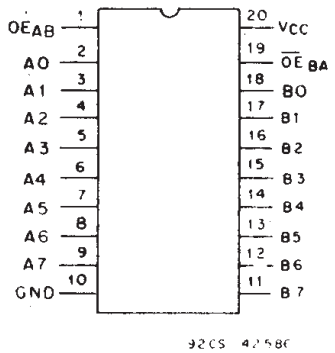


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**TERMINAL ASSIGNMENT**

# CD54/74AC623
# CD54/74ACT623

**STATIC ELECTRICAL CHARACTERISTICS: AC Series**

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage $V_{IH}$ | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V |
| | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | |
| | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | |
| Low-Level Input Voltage $V_{IL}$ | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V |
| | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | |
| | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | |
| High-Level Output Voltage $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | -0.05 | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | -4 | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | #, * | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 0.05 | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | 12 | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | #, * | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current $I_I$ | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| 3-State Leakage Current $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O$ = $V_{CC}$ or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply Current, MSI $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

**STATIC ELECTRICAL CHARACTERISTICS: ACT Series**

| CHARACTERISTICS | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | $V_I$ (V) | $I_O$ (mA) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| High-Level Input Voltage $V_{IH}$ | | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V |
| Low-Level Input Voltage $V_{IL}$ | | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V |
| High-Level Output Voltage $V_{OH}$ | $V_{IH}$ or $V_{IL}$ #, * | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| Low-Level Output Voltage $V_{OL}$ | $V_{IH}$ or $V_{IL}$ #, * | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| Input Leakage Current $I_I$ | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| 3-State Leakage Current $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O$ = $V_{CC}$ or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| Quiescent Supply Current, MSI $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load $\Delta I_{CC}$ | $V_{CC}$-2.1 | | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA |

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

**ACT INPUT LOADING TABLE**

| INPUT | UNIT LOAD* |
|---|---|
| An, Bn | 0.83 |
| $\overline{OE}_{BA}$ | 0.64 |
| $OE_{AB}$ | 0.15 |

*Unit load is $\Delta I_{CC}$ limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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# CD54/74AC623
# CD54/74ACT623

**SWITCHING CHARACTERISTICS: AC Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Output | $t_{PLH}$ $t_{PHL}$ | 1.5<br>3.3*<br>5† | —<br>3.5<br>2.5 | 108<br>12.2<br>8.7 | —<br>3.4<br>2.4 | 120<br>13.4<br>9.6 | ns |
| Output Disable to Output | $t_{PLZ}$ $t_{PHZ}$ | 1.5<br>3.3<br>5 | —<br>4.8<br>3.5 | 153<br>17.1<br>12.2 | —<br>4.7<br>3.4 | 168<br>18.8<br>13.4 | ns |
| Output Enable to Output | $t_{PZL}$ $t_{PZH}$ | 1.5<br>3.3<br>5 | —<br>4.8<br>3.5 | 153<br>17.1<br>12.2 | —<br>4.7<br>3.4 | 168<br>18.8<br>13.4 | ns |
| Power Dissipation Capacitance | $C_{PD}$§ | — | 66 Typ. | | 66 Typ. | | pF |
| Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | $C_I$ | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | $C_O$ | — | — | 15 | — | 15 | pF |

**SWITCHING CHARACTERISTICS: ACT Series; $t_r$, $t_f$ = 3 ns, $C_L$ = 50 pF**

| CHARACTERISTICS | SYMBOL | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| Propagation Delays: Data to Output | $t_{PLH}$ $t_{PHL}$ | 5† | 2.7 | 9.6 | 2.7 | 10.6 | ns |
| Output Disable to Output | $t_{PLZ}$ $t_{PHZ}$ | 5 | 3.7 | 13.1 | 3.6 | 14.4 | ns |
| Output Enable to Output | $t_{PZH}$ $t_{PZL}$ | 5 | 3.7 | 13.1 | 3.6 | 14.4 | ns |
| Power Dissipation Capacitance | $C_{PD}$§ | — | 66 Typ. | | 66 Typ. | | pF |
| Min. (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ See Fig. 1 | 5 | 4 Typ. @ 25°C | | | | V |
| Max. (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ See Fig. 1 | 5 | 1 Typ. @ 25°C | | | | V |
| Input Capacitance | $C_I$ | — | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | $C_O$ | — | — | 15 | — | 15 | pF |

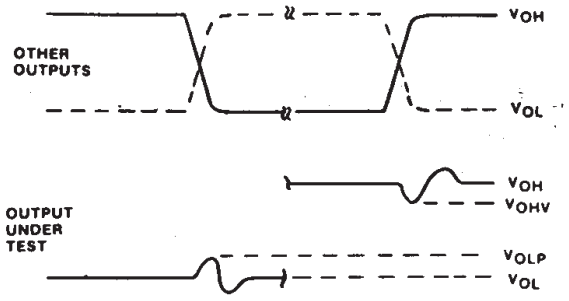
*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§$C_{PD}$ is used to determine the dynamic power consumption, per channel.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where $f_i$ = input frequency
$C_L$ = output load capacitance
$V_{CC}$ = supply voltage.

# CD54/74AC623
# CD54/74ACT623

## PARAMETER MEASUREMENT INFORMATION




NOTES:
1. $V_{OHV}$ AND $V_{OLP}$ ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, $t_r$ = 3 ns, $t_f$ = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

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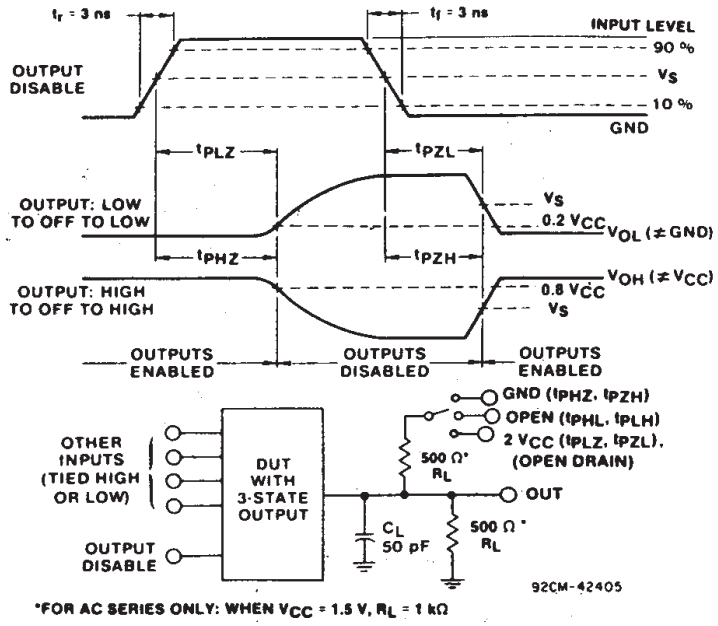
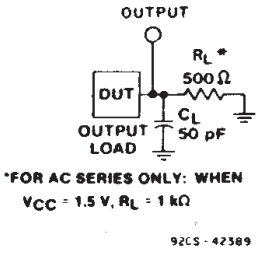
*Fig. 1 - Simultaneous switching transient waveforms.*




*FOR AC SERIES ONLY: WHEN $V_{CC}$ = 1.5 V, $R_L$ = 1 kΩ

*Fig. 2 - Three-state propagation delay times and test circuit.*



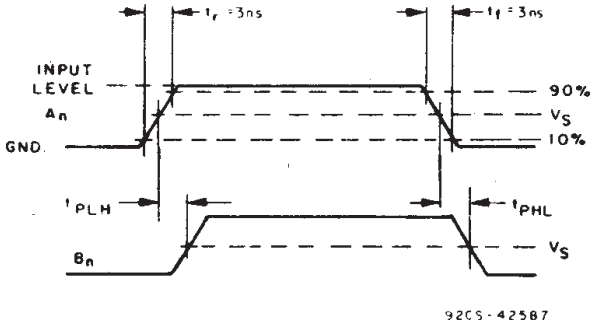




*Fig. 3 - Propagation delay times and test circuit.*

| | CD54/74AC | CD54/74ACT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| Input Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 1.5 V |
| Output Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 0.5 $V_{CC}$ |

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD54ACT623F3A | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD54ACT623F3A | Samples |
| CD74AC623E | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC623E | Samples |
| CD74AC623M | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC623M | Samples |
| CD74ACT623M96 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT623M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54ACT623, CD74ACT623 :**

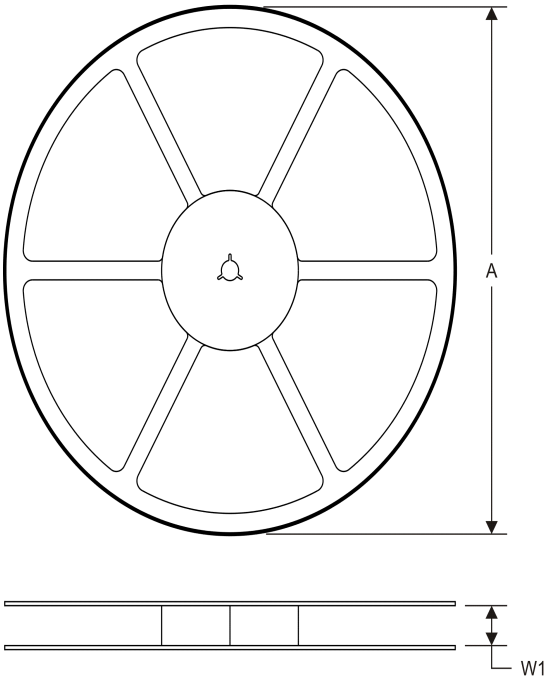
- Catalog: CD74ACT623
- Military: CD54ACT623

NOTE: Qualified Version Definitions:

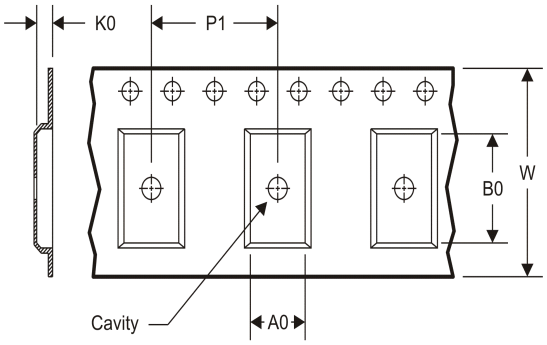
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



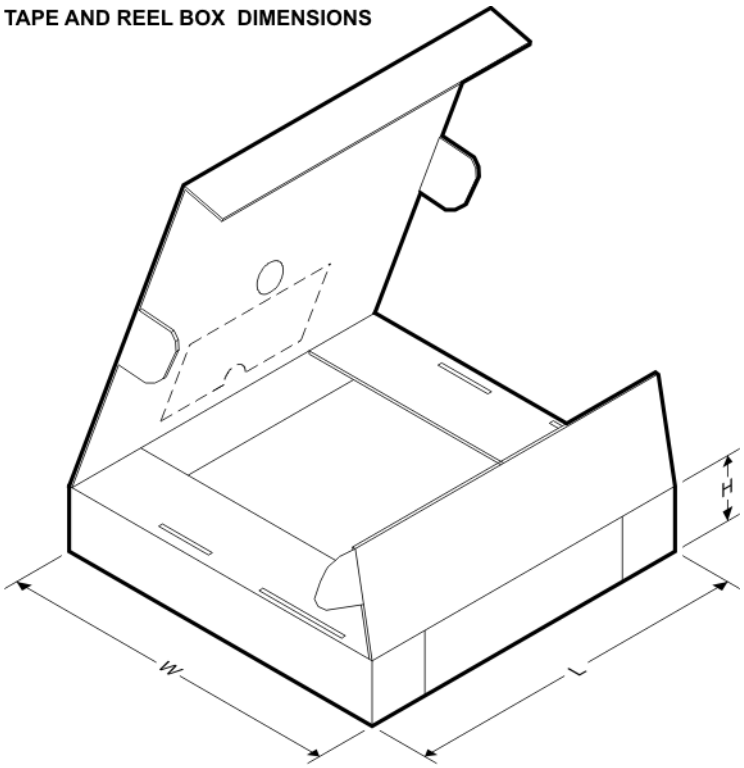

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74ACT623M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



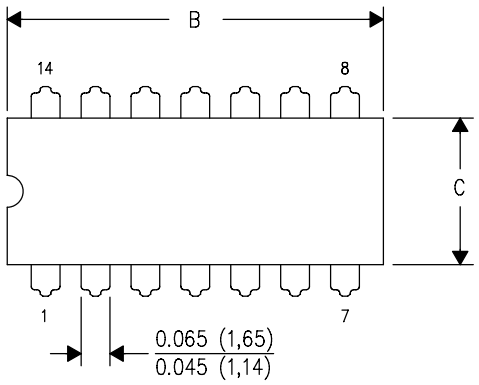

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74ACT623M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

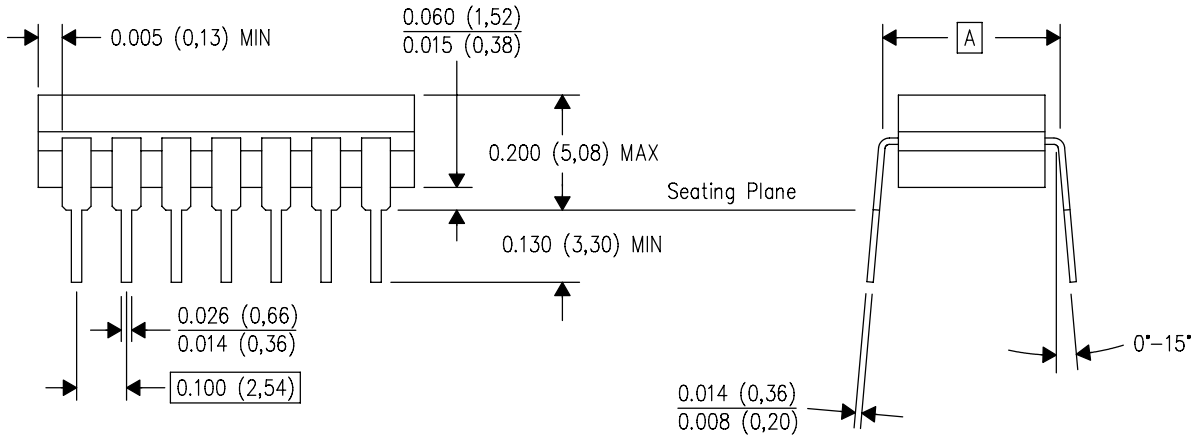
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



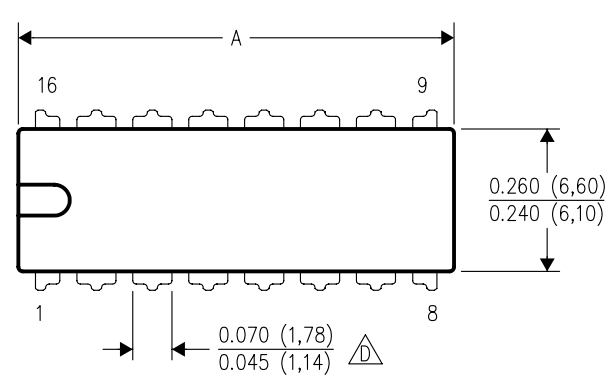

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

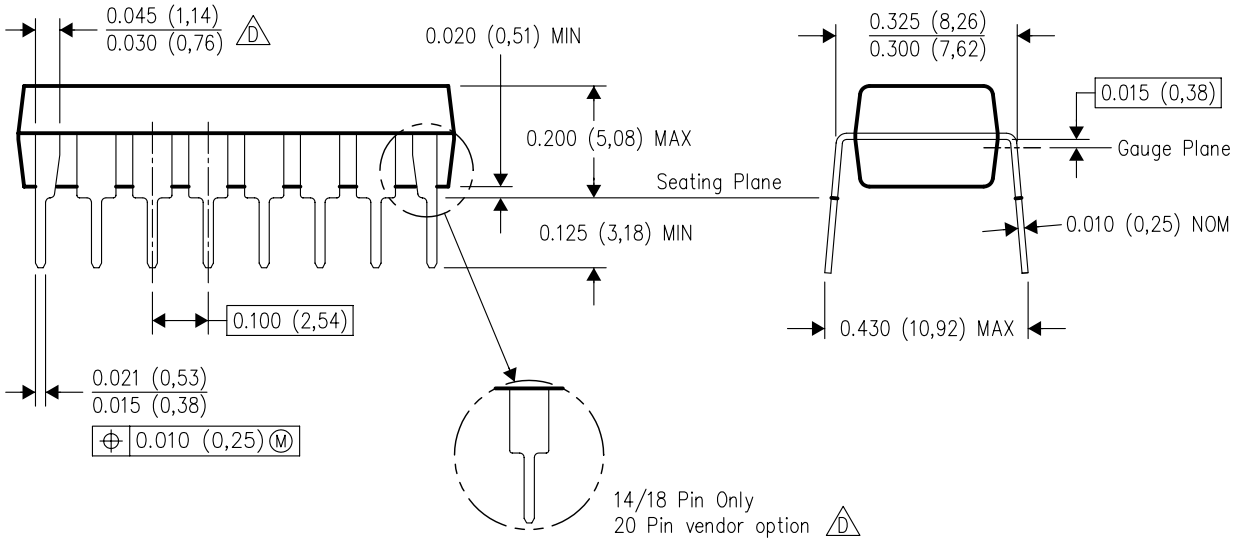
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



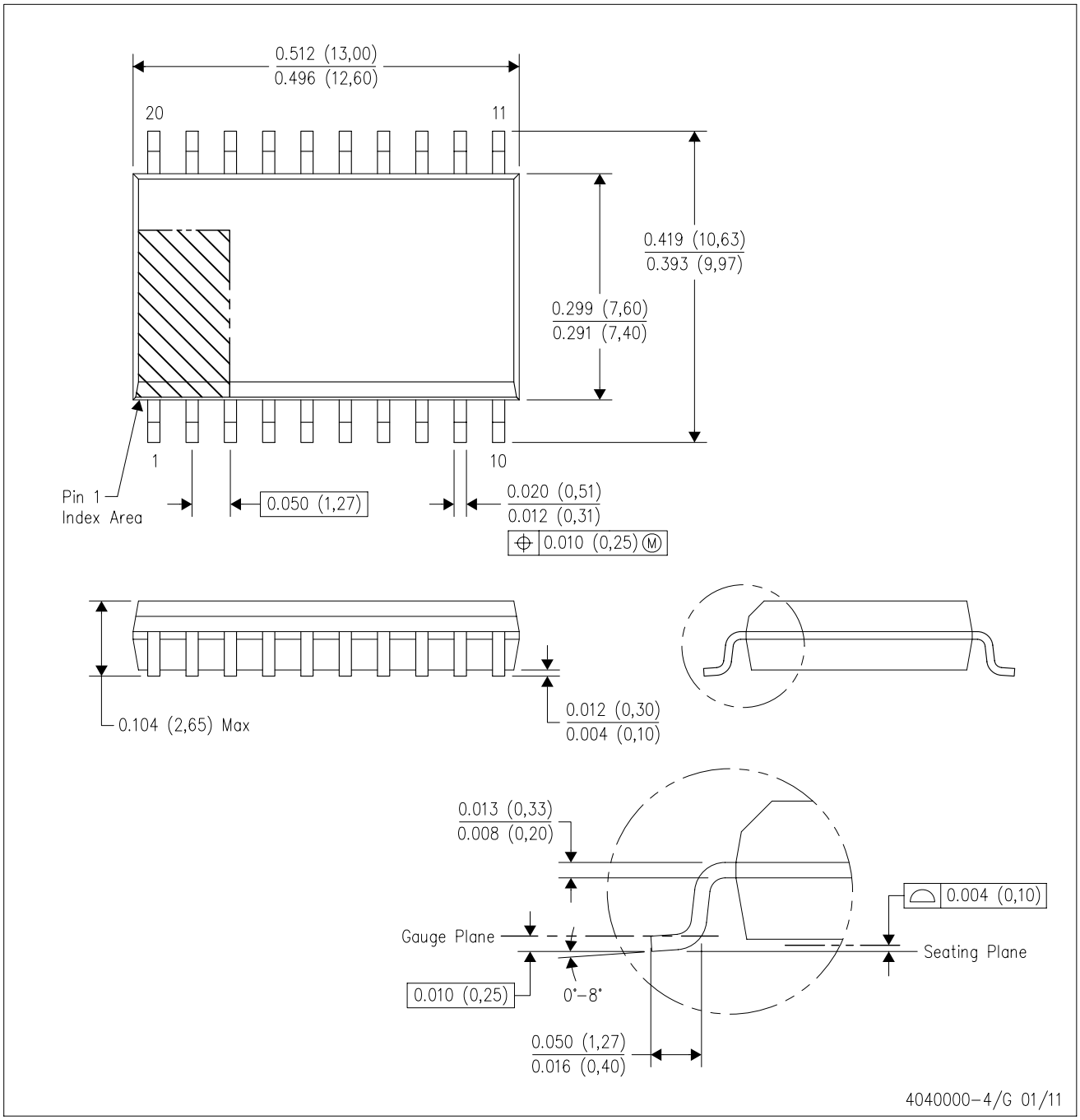

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

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